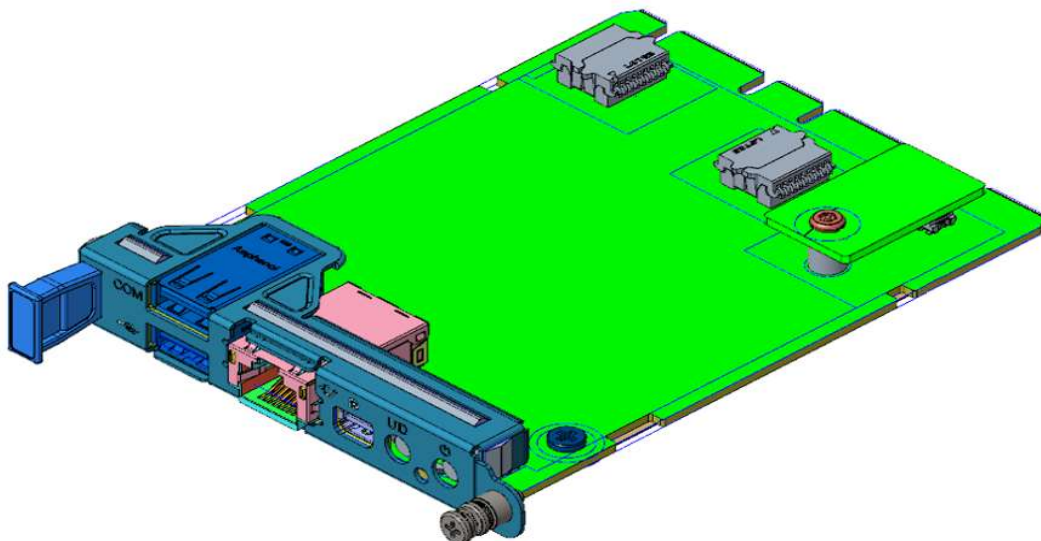


Cloudflare - Lenovo DC-SCM2.0

Pin Definition



Revision: 2.0
Date: 2023/3/20

CSP Development, DCG, Lenovo

Side A	Single Node Primary/Alternative Function (If Applicable)	Voltage Single/Dual	Direction DC-SCM View	Cloudflare DC-SCM2.0 Net Name	Description
OA1	GND			GND	
OA2	PCIE_HPMROOT_SCM_HPM_0_DN / USB3_SCMHOST2_SCM_HPM_DN		output / output	NC_PCIE_HPMROOT_SCM_HPM_0_DN	NC on DC-SCM, PCIe x4
OA3	PCIE_HPMROOT_SCM_HPM_0_DP / USB3_SCMHOST2_SCM_HPM_DP		output / output	NC_PCIE_HPMROOT_SCM_HPM_0_DP	
OA4	GND			GND	
OA5	PCIE_HPMROOT_SCM_HPM_1_DN / LTP12_SCM_HPM_CLK_DN / DISPLAYPORT_SCM_HPM_LANE0_DN	PCie / LTP1 / DP	output/ output/ output	NC_PCIE_HPMROOT_SCM_HPM_1_DN	NC on DC-SCM, PCIe x4
OA6	PCIE_HPMROOT_SCM_HPM_1_DP / LTP12_SCM_HPM_CLK_DP / DISPLAYPORT_SCM_HPM_LANE0_DP	PCie / LTP1 / DP	output/ output/ output	NC_PCIE_HPMROOT_SCM_HPM_1_DP	
OA7	GND			GND	
OA8	PCIE_HPMROOT_SCM_HPM_2_DN / SGMII_SCM_HPM_DN		output / output	NC_PCIE_HPMROOT_SCM_HPM_2_DN	NC on DC-SCM, PCIe x4
OA9	PCIE_HPMROOT_SCM_HPM_2_DP / SGMII_SCM_HPM_DP		output / output	NC_PCIE_HPMROOT_SCM_HPM_2_DP	
OA10	GND			GND	
OA11	PCIE_HPMROOT_SCM_HPM_3_DN / LTP12_SCM_HPM_DATA_DN / DISPLAYPORT_SCM_HPM_LANE1_DN	PCie / LTP1 / DP	output / output/ output	NC_PCIE_HPMROOT_SCM_HPM_3_DN	NC on DC-SCM, PCIe x4
OA12	PCIE_HPMROOT_SCM_HPM_3_DP / LTP12_SCM_HPM_DATA_DP / DISPLAYPORT_SCM_HPM_LANE1_DP	PCie / LTP1 / DP	output / output/ output	NC_PCIE_HPMROOT_SCM_HPM_3_DP	
OA13	GND			GND	
OA14	PECI_HPM_SCM / GPIO	0.85-1.21	inout	PECI_BMC	PECI for Intel platform
A1	P12V_AUX		input	P12V_SCM_AUX	12V Power
A2	P12V_AUX		input	P12V_SCM_AUX	
A3	P12V_AUX		input	P12V_SCM_AUX	
A4	P12V_AUX		input	P12V_SCM_AUX	
A5	GND			GND	
A6	GND			GND	
A7	PRSN11_HPM_SCM_N	0	input	PRSN11_N	Discovery/Sequencing, Present Pin 1
A8	JTAG_SCMCNTRL_TCK	3.3	output	HPM_JTAG_TCK	JTAG
A9	JTAG_SCMCNTRL_TDI	3.3	input	HPM_JTAG_TDI	
A10	JTAG_SCMCNTRL_TDO	3.3	output	HPM_JTAG_TDO	
A11	JTAG_SCMCNTRL_TMS	3.3	output	HPM_JTAG_TMS	
A12	JTAG_SCMCNTRL_TRST_N	3.3	output	HPM_JTAG_TRST_N	
A13	SCM_HPM_STBY_RST_N	3.3	output	PFR_HPM_STBY_RST_N	Discovery/Sequencing, System Reset
A14	SCM_HPM_STBY_EN	3.3	output	HPM_STBY_EN	Discovery/Sequencing, HPM Standby PWR Enable
A15	I2C_3V3_0_SCL	3.3	inout	DCSCI_BMC_I2C_R_SCL11	I2C, 3.3V. HPM FRU must be I2C0.
A16	I2C_3V3_0_SDA	3.3	inout	DCSCI_BMC_I2C_R_SDA11	
A17	I2C_3V3_1_SCL	3.3	inout	DCSCI_I2C_3V3_SCL7_ROT	I2C, 3.3V. For HSBB via RoT I2C Filter.
A18	I2C_3V3_1_SDA	3.3	inout	DCSCI_I2C_3V3_SDA7_ROT	
A19	GND			GND	
A20	LTP1_SCM_HPM_DATA_DN		output	LTP1_SCM_HPM_DATA_DN	LTP1, SCM to HPM
A21	LTP1_SCM_HPM_DATA_DP		output	LTP1_SCM_HPM_DATA_DP	
A22	GND			GND	
A23	LTP1_SCM_HPM_CLK_DN		output	LTP1_SCM_HPM_CLK_DN	LTP1, SCM to HPM
A24	LTP1_SCM_HPM_CLK_DP		output	LTP1_SCM_HPM_CLK_DP	
A25	GND			GND	
A26	I2C_3V3_2_SCL	3.3	inout	DCSCI_I2C_3V3_SCL9_ROT	I2C, 3.3V. For CPU VRs via RoT I2C Filter.
A27	I2C_3V3_2_SDA	3.3	inout	DCSCI_I2C_3V3_SDA9_ROT	
A28	PCIE_HPM_SCM_PERST_N	3.3	input	PCIE_HPM_SCM_PERST_N	PCIe Reset
A29	GND			GND	
A30	PCIE_HPMROOT_SCM_HPM_4_DN		output	PCIE_HPMROOT_SCM_HPM_RX_C_DN	PCIe x1, Connect to BMC PCIe EP for Video
A31	PCIE_HPMROOT_SCM_HPM_4_DP		output	PCIE_HPMROOT_SCM_HPM_RX_C_DP	
A32	GND			GND	
A33	PCIE_SCMROOT_SCM_HPM_DN / USB3_SCMHOST1_SCM_HPM_DN		output / output	PCIE_SCMROOT_SCM_HPM_TX_C_DN	PCIe x1, Connect to BMC PCIe RC (Reserved)
A34	PCIE_SCMROOT_SCM_HPM_DP / USB3_SCMHOST1_SCM_HPM_DP		output / output	PCIE_SCMROOT_SCM_HPM_TX_C_DP	
A35	GND			GND	
A36	PCIE_HPM_SCM_CLK_100M_0_DN		input	PCIE_HPM_SCM_CLK_100M_0_DN	PCIe Clock to BMC PCIe EP, Connect to BMC
A37	PCIE_HPM_SCM_CLK_100M_0_DP		input	PCIE_HPM_SCM_CLK_100M_0_DP	
A38	GND			GND	
A39	I2C_I3C_1V0_18_SCL / FSI_1V2_0_SCL	1.0/1.2	inout	DCSCI_I3C_1V0_SCL1	I3C, 1.0V
A40	I2C_I3C_1V0_18_SDA / FSI_1V2_0_SDA	1.0/1.2	inout	DCSCI_I3C_1V0_SDA1	
A41	I2C_I3C_1V0_19_SCL / FSI_1V2_1_SCL	1.0/1.2	inout	DCSCI_I3C_1V0_SCL2	I3C, 1.0V
A42	I2C_I3C_1V0_19_SDA / FSI_1V2_1_SDA	1.0/1.2	inout	DCSCI_I3C_1V0_SDA2	
A43	I2C_3V3_3_SCL	3.3 (Single) 1.8 (Dual)	inout	DCSCI_BMC_I2C_R_SCL12	I2C, 3.3V
A44	I2C_3V3_3_SDA	3.3 (Single) 1.8 (Dual)	inout	DCSCI_BMC_I2C_R_SDA12	
A45	I2C_3V3_4_SCL	3.3 (Single) 1.8 (Dual)	inout	DCSCI_BMC_I2C_R_SCL10	I2C, 3.3V
A46	I2C_3V3_4_SDA	3.3 (Single) 1.8 (Dual)	inout	DCSCI_BMC_I2C_R_SDA10	
A47	I2C_3V3_5_SCL	3.3 (Single) 1.8 (Dual)	inout	DCSCI_BMC_I2C_R_SCL5	I2C, 3.3V
A48	I2C_3V3_5_SDA	3.3 (Single) 1.8 (Dual)	inout	DCSCI_BMC_I2C_R_SDA5	
A49	I2C_3V3_6_SCL	3.3 (Single) 1.8 (Dual)	inout	DCSCI_I2C_3V3_SCL6_ROT	I2C, 3.3V. For PMBus via RoT I2C Filter.
A50	I2C_3V3_6_SDA	3.3 (Single) 1.8 (Dual)	inout	DCSCI_I2C_3V3_SDA6_ROT	
A51	I2C_I3C_1V8_16_SCL	1.8	inout	DCSCI_BMC_I2C_R_SCL3_1V8	I2C, 1.8V
A52	I2C_I3C_1V8_16_SDA	1.8	inout	DCSCI_BMC_I2C_R_SDA3_1V8	
A53	GND			GND	
A54	SPI_HPMCNTRL_TPM_CLK / I2C_I3C_1V8_10_SCL	1.8	input / inout	SPI_TPM_CLK	TPM SPI
A55	SPI_HPMCNTRL_TPM_CS_N / I2C_I3C_1V8_10_SDA / QSPI_HPMCNTRL_TPM_CS_N	1.8	input / inout / input	SPI_TPM_CS_N	
A56	SPI_HPMCNTRL_TPM_MOSI / I2C_I3C_1V8_11_SCL	1.8	input / inout	SPI_TPM_MOSI	
A57	SPI_HPMCNTRL_TPM_MISO / I2C_I3C_1V8_11_SDA	1.8	output / inout	SPI_TPM_MISO	
A58	I2C_I3C_1V8_12_SCL	1.8	inout	DCSCI_I2C_SCL_ROT_1V8	
A59	I2C_I3C_1V8_12_SDA	1.8	inout	DCSCI_I2C_SDA_ROT_1V8	I2C, 1.8V From RoT to CPU which is used for CPU I2C Mailbox
A60	GPI / SPI_SCMCNTRL_IRQ0_N	1.8	input / input	SPI_HPM_SCM_IRQ0_N	SPI_IRQ#
A61	I2C_I3C_1V8_13_SCL	1.8	inout	DCSCI_I2C8_SCL_1V8	I2C, 1.8V
A62	I2C_I3C_1V8_13_SDA	1.8	inout	DCSCI_I2C8_SDA_1V8	
A63	UART0_HPM_SCM_DATA / GPIO	3.3	input / input	UART0_HPM_SCM_DATA	BMC UART1 RX (from DC-SCM View)
A64	GND			GND	
A65	PCIE_HPMROOT_SCM_HPM_5_DN		output	NC_PCIE_HPMROOT_SCM_HPM_5_DN	PCIe x1 for USB 3.0 Controller
A66	PCIE_HPMROOT_SCM_HPM_5_DP		output	NC_PCIE_HPMROOT_SCM_HPM_5_DP	
A67	GND			GND	NC on DC-SCM
A68	PCIE_HPM_SCM_CLK_100M_1_S0_DN / PCIE_HPM_SCM_CLK_100M_1_S5_DN		input / input	PCIE_HPM_SCM_CLK_100M_1_S0_DN	PCIe Clock to BMC PCIe RC, Connect to BMC
A69	PCIE_HPM_SCM_CLK_100M_1_S0_DP / PCIE_HPM_SCM_CLK_100M_1_S5_DP		input / input	PCIE_HPM_SCM_CLK_100M_1_S0_DP	
A70	GND			GND	

Note1: 3.3/BAT mean 3.3V when AC is applied and 3.0 BAT in G3

Side B	Single Node Primary/Alternative Function (if Applicable)	Voltage Single/Dual	Direction DC-SCM View	Cloudflare DC-SCM2.0 Net Name	Description
OB1	GND			GND	
OB2	PCIE_HPMROOT_HPM_SCM_0_DN / USB3_SCMHOST2_HPM_SCM_DN		input / input	NC_PCIE_HPMROOT_HPM_SCM_0_DN	NC on DC-SCM, PCIe x4
OB3	PCIE_HPMROOT_HPM_SCM_0_DP / USB3_SCMHOST2_HPM_SCM_DP		input / input	NC_PCIE_HPMROOT_HPM_SCM_0_DP	
OB4	GND			GND	
OB5	PCIE_HPMROOT_HPM_SCM_1_DN / LTP12_HPM_SCM_CLK_DN / DISPLAYPORT_AUX_DN	PCIE / LTP1 / DP	input / input / inout	NC_PCIE_HPMROOT_HPM_SCM_0_DN	NC on DC-SCM, PCIe x4
OB6	PCIE_HPMROOT_HPM_SCM_1_DP / LTP12_HPM_SCM_CLK_DP / DISPLAYPORT_AUX_DP	PCIE / LTP1 / DP	input / input / inout	NC_PCIE_HPMROOT_HPM_SCM_0_DP	
OB7	GND			GND	
OB8	PCIE_HPMROOT_HPM_SCM_2_DN / SGMII_HPM_SCM_DN		input / input	NC_PCIE_HPMROOT_HPM_SCM_0_DN	NC on DC-SCM, PCIe x4
OB9	PCIE_HPMROOT_HPM_SCM_2_DP / SGMII_HPM_SCM_DP		input / input	NC_PCIE_HPMROOT_HPM_SCM_0_DP	
OB10	GND			GND	
OB11	PCIE_HPMROOT_HPM_SCM_3_DN / LTP12_HPM_SCM_DATA_DN / USB2_SCMHOST3_DN	PCIE / LTP1 / USB2	input / input / inout	NC_PCIE_HPMROOT_HPM_SCM_0_DN	NC on DC-SCM, PCIe x4
OB12	PCIE_HPMROOT_HPM_SCM_3_DP / LTP12_HPM_SCM_DATA_DP / USB2_SCMHOST3_DP	PCIE / LTP1 / USB2	input / input / inout	NC_PCIE_HPMROOT_HPM_SCM_0_DP	
OB13	GND			GND	
OB14	PECI_VREF_HPM_SCM / GPI	0.85-1.21	input	PVCCIO_PECI	PECI Power
B1	ESPI_HPMCNTL_CLK	1.8	input	ESPI_HPMCNTL_CLK	ePSI Connect to BMC
B2	ESPI_HPMCNTL_CS0_N	1.8	input	ESPI_HPMCNTL_CS0_N	
B3	ESPI_HPMCNTL_RESET_N	1.8	input	ESPI_HPMCNTL_RESET_N	
B4	ESPI_HPMCNTL_IO_0	1.8	inout	ESPI_HPMCNTL_IO_0	
B5	ESPI_HPMCNTL_IO_1	1.8	inout	ESPI_HPMCNTL_IO_1	
B6	ESPI_HPMCNTL_IO_2	1.8	inout	ESPI_HPMCNTL_IO_2	
B7	ESPI_HPMCNTL_IO_3	1.8	inout	ESPI_HPMCNTL_IO_3	
B8	ESPI_HPMCNTL_ALERT0_N	1.8	output	ESPI_HPMCNTL_ALERT0_N	I2C, 1.8V
B9	I2C_I3C_1V8_17_SCL / ESPI0_HPMCNTL_CS1_N	1.8	inout / input	DCSCI_BMC_I2C_R_SCL4_1V8	
B10	I2C_I3C_1V8_17_SDA / ESPI0_HPMCNTL_ALERT1_N	1.8	inout / output	DCSCI_BMC_I2C_R_SDA4_1V8	
B11	GND			GND	HPM Boot QSPI
B12	QSPI_HPMCNTL_CLK	1.8	input	SYS_QSPI_CLK_1V8	
B13	QSPI_HPMCNTL_CS0_N	1.8	input	SYS_QSPI_CS0_1V8_N	
B14	QSPI_HPMCNTL_IO_0	1.8	inout	SYS_QSPI_D0_1V8	
B15	QSPI_HPMCNTL_IO_1	1.8	inout	SYS_QSPI_D1_1V8	
B16	QSPI_HPMCNTL_IO_2	1.8	inout	SYS_QSPI_D2_1V8	
B17	QSPI_HPMCNTL_IO_3	1.8	inout	SYS_QSPI_D3_1V8	
B18	QSPI_HPMCNTL_CS1_N / GPI	1.8	input / input	SYS_QSPI_CS1_1V8_N	LTP1, HPM to SCM
B19	GND			GND	
B20	LTP1_HPM_SCM_DATA_DN		input	LTP1_HPM_SCM_DATA_DN	
B21	LTP1_HPM_SCM_DATA_DP		input	LTP1_HPM_SCM_DATA_DP	LTP1, HPM to SCM
B22	GND			GND	
B23	LTP1_HPM_SCM_CLK_DN		input	LTP1_HPM_SCM_CLK_DN	
B24	LTP1_HPM_SCM_CLK_DP		input	LTP1_HPM_SCM_CLK_DP	Discovery/Sequencing, HPM Standby Ready Intrusion
B25	GND			GND	
B26	HPM_SCM_STBY_RDY	3.3	input	HPM_STBY_RDY	
B27	HPM_SCM_INTRUSION_N	3.3/BAT	input	FM_INTRUDER_BMC_N	Battery Power
B28	P3V0_HPM_SCM_BAT	3.0 BAT	input	P3V0_HPM_SCM_BAT	
B29	GND			GND	PCIe x1, Connect to BMC PCIe EP for Video
B30	PCIE_HPMROOT_HPM_SCM_4_DN		input	PCIE_HPMROOT_HPM_SCM_TX_DN	
B31	PCIE_HPMROOT_HPM_SCM_4_DP		input	PCIE_HPMROOT_HPM_SCM_TX_DP	
B32	GND			GND	PCIe x1, Connect to BMC PCIe RC (Reserved)
B33	PCIE_SCMROOT_HPM_SCM_DN / USB3_SCMHOST1_HPM_SCM_DN		input / input	PCIE_SCMROOT_HPM_SCM_RX_DN	
B34	PCIE_SCMROOT_HPM_SCM_DP / USB3_SCMHOST1_HPM_SCM_DP		input / input	PCIE_SCMROOT_HPM_SCM_RX_DP	
B35	GND			GND	HPM USB Host to DC-SCM Panel IO USB TypeA Connector
B36	USB2_SCMHOST1_DN / USB2_HPMHOST1_DN / GPIO	3.3	inout / inout	USB2_HPMHOST1_DN	
B37	USB2_SCMHOST1_DP / USB2_HPMHOST1_DP / GPIO	3.3	inout / inout	USB2_HPMHOST1_DP	
B38	GND			GND	I3C, 1.8V, from BMC/ROT to CPU, reserved for CPU attestation on Intel platform.
B39	I2C_I3C_1V8_14_SCL	1.8	inout	DCSCI_ROTBMCI3C_SCL1_1V8	
B40	I2C_I3C_1V8_14_SDA	1.8	inout	DCSCI_ROTBMCI3C_SDA1_1V8	
B41	I2C_I3C_1V8_15_SCL	1.8	inout	DCSCI_BMC_I2C_R_SCL2_1V8	
B42	I2C_I3C_1V8_15_SDA	1.8	inout	DCSCI_BMC_I2C_R_SCL1_1V8	I2C, 1.8V
B43	NCSI_HPM_SCM_CLK / GPIO	3.3	input	NCSI_CLK	NCSI
B44	NCSI_HPM_SCM_CRS_DV / GPIO	3.3	input	NCSI_CRS_DV	
B45	NCSI_SCM_HPM_TX_EN / GPIO	3.3	output	NCSI_TXEN	
B46	NCSI_SCM_HPM_D0 / GPIO	3.3	output	NCSI_TXD0	
B47	NCSI_SCM_HPM_D1 / GPIO	3.3	output	NCSI_TXD1	
B48	NCSI_HPM_SCM_D0 / GPIO	3.3	input	NCSI_RXD0	
B49	NCSI_HPM_SCM_D1 / GPIO	3.3	input	NCSI_RXD1	For HPM FRU PWR
B50	VCC_SCM_HPM_FRU	3.3	output	VCC_SCM_HPM_FRU	
B51	UART0_SCM_HPM_DATA / PCIE_SCM_HPM_PERST_N / GPO/ NCSI2_SCM_HPM_TX_EN	3.3	output / output / output	UART0_SCM_HPM_DATA	BMC UART1 TX (from DC-SCM View)
B52	I2C_3V3_7_SCL / SGPIO_CLK / NCSI2_HPM_SCM_CLK	3.3	inout / output / output	SGPIO_SCM_HPM_CLK	SGPIO
B53	I2C_3V3_7_SDA / SGPIO_ID / NCSI2_HPM_SCM_CRS_DV	3.3	inout / output / output	SGPIO_SCM_HPM_ID	
B54	I2C_3V3_8_SCL / SGPIO_DATAOUT / NCSI2_SCM_HPM_D0	3.3	inout / output / inout	SGPIO_SCM_HPM_DATAOUT	
B55	I2C_3V3_8_SDA / SGPIO_DATAIN / NCSI2_SCM_HPM_D1	3.3	inout / input / input	SGPIO_SCM_HPM_DATAIN	
B56	I2C_3V3_9_SCL / UART1_SCM_HPM_DATA / NCSI2_HPM_SCM_D0	3.3	inout / output / inout	UART2_TX_SCM_HPM_DATA	BMC UART2 TX (from DC-SCM View)
B57	I2C_3V3_9_SDA / UART1_HPM_SCM_DATA / NCSI2_HPM_SCM_D1	3.3	inout / input / input	UART2_RX_SCM_HPM_DATA	BMC UART2 RX (from DC-SCM View)
B58	PRSENT0_SCM_HPM_N	0	output	PRSENT0_N	Present Pin 0
B59	SPI_SCMCNTRL_CS1_N / GPIO	3.3	output / inout	PWR_BTN_N (GPIO)	PWR BTN from DC-SCM to HPM
B60	SPI_SCMCNTRL_CLK	3.3	output	SPI_SCMCNTRL_CLK	SPI_SCMCNTRL, DC-SCM is the Initiator
B61	SPI_SCMCNTRL_MISO	3.3	input	SPI_SCMCNTRL_MISO	
B62	SPI_SCMCNTRL_MOSI	3.3	output	SPI_SCMCNTRL_MOSI	
B63	SPI_SCMCNTRL_CS0_N	3.3	output	SPI_SCMCNTRL_CS0_N	
B64	GND			GND	PCIe x1 for USB 3.0 Controller NC on DC-SCM
B65	PCIE_HPMROOT_HPM_SCM_5_DN		input	NC_PCIE_HPMROOT_HPM_SCM_5_DN	
B66	PCIE_HPMROOT_HPM_SCM_5_DP		input	NC_PCIE_HPMROOT_HPM_SCM_5_DP	
B67	GND			GND	To BMC USB A
B68	USB2_SCMHOST2_DN / USB2_HPMHOST2_DN / GPIO	3.3	inout / inout	USB2_HPMHOST2_DN	
B69	USB2_SCMHOST2_DP / USB2_HPMHOST2_DP / GPIO	3.3	inout / inout	USB2_HPMHOST2_DP	
B70	GND			GND	